REMARKS

Attached hereto is an Excess Claims Letter and fee for one excess independent claim.

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-20 are all of the claims pending in the present Application. New claims 17-20 have been added. The Examiner has withdrawn claims 12 and 16 from current consideration as addressing a separate invention from that described by claims 1-11 and 13-15. Applicants respectfully traverse that this Restriction Requirement is proper when the invention is properly understood in view of the cited prior art. The new claims further highlight the interconnection between the Examiner's categorization of claims as based upon a subcombination rationale.

Claims 1, 4, 7, 11, and 13-15 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,234,440 to Tao. Claims 1, 2, 4, 5, 7, 9, 11, and 13-15 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,372,651 to Yang. Claims 1, 2, 4, 7, 11, and 13-15 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,107,172 to Yang. Claims 1, 2, 4, 7, 11, and 13-15 stand rejected under 35 USC §102(e) as anticipated by US Patent 6,283,131 to Chen.

Claims 3, 5, 6, and 8-10 stand rejected under 35 USC §103(a) as unpatentable over Tao or Chen, further in view of US Patent 5,940,719 to Jang. Claims 3 and 8 stand rejected under 35 USC §103(a) as unpatentable over Yang (US Patent 6,107,172), further in view of Jang. Claims 6 and 10 stand rejected under 35 USC §103(a) as unpatentable over Chen, further in view of US Patent Application Publication US 2001/0009792 to Bothra et al.

These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, the present invention is directed to a method of fabricating an electronic chip on a wafer. A first mask at a predetermined lower resolution is developed on a surface of a wafer. The first mask is etched under a first set of conditions for a predetermined period to achieve a higher resolution mask. The higher resolution is 100 nm or less.

II. THE RESTRICTION REQUIREMENT

As best understood, the Examiner has classified the claims into two categories, which the Examiner considers as being two "*subcombinations usuable together in a single combination.*" The Examiner continues: "*The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention II has separate utility such as a method for controlling the line width variation tolerances of isolated and nested features during the manufacture of a semiconductor device using a single etch step (i.e., in the absence of a (first) trim etch step). See MPEP§ 806.05(d).*

Applicants respectfully submit that there are at least three problems with this analysis under MPEP§ 806.05(d). First, Applicants submit that the Examiner incorrectly interprets the restriction requirement described in MPEP§ 806.05(d). "Two subcombinations" would inherently require a combination/subcombination relationship to be identified somewhere in the claim structure. Here, the Examiner has only two claim categories, both of which are classified as subcombinations. That is, the Examiner's current evaluation identifies no combination for which the two categories become subcombinations.

Second, in order to achieve resolution at or below 100nm in a wafer fabrication, the fabrication process must be able to achieve a satisfactory manufacturing parameter called Across Chip Linewidth Variation (ACLV). As explained on page 2 of the specification, this parameter is closely associated with the etching success for isolated features versus nested features. Applicants have amended the claims and have added new claims 17-20 to clarify, for the Examiner's benefit, how ACLV is related to the original language of the claims and to the method of obtaining a critical dimension below 100 nm.

Stated slightly differently, what claim 12 articulates relative to independent claims 1, 7, and 11 is that the prior art etch recipes upon which the Examiner relies upon are insufficient to provide a chip critical dimension at 100 nm or less unless that etch recipe additionally provides a mechanism that ensures that all lines across the circuit are consistently etched. Without this additional constraint, the etching process will fail to provide a circuit both that functions and that has all lines within the critical dimension of 100 nm or less. That is, if the circuit functions, some lines will be above 100 nm; if all lines are below 100 nm, there will be lines or components in the circuit that are over-etched, thereby yielding a chip having a non-functioning circuit when the target critical dimension is as small as 100 nm.

Third, in accordance with the final paragraph of MPEP§ 806.05(d), Applicants have amended claim 12 to clarify that the utility of this technique, as claimed, applies for chip resolutions below 100nm, thereby rendering the Examiner's argument moot. That is, Applicants consider it irrelevant that the technique of claim 12 is used above 100nm, since it is clear from the prior art references that any of various alternate etching recipes would achieve an etch adequate for a critical dimension greater than 100 nm.

Forth, Applicants additionally point out that the amendment to claim 12 becomes significant for a combination/subcombination analysis under MPEP§ 806.05(c), since the Examiner does not provide a reasonable reference demonstrating any technique for achieving a critical dimension at or below 100 nm, let alone one that relies upon RF tuning to provide the capability of achieving an adequate ACLV.

Applicants, accordingly, respectfully request that the Examiner reconsider and withdraw this Restriction Requirement.

III. THE PRIOR ART REJECTIONS

The Examiner asserts that claims 1, 4, 7, 11, and 13-15 are anticipated by US Patent 6,234,440 to Tao, that claims 1, 2, 4, 5, 7, 9, 11, and 13-15 are anticipated by US Patent 6,372,651 to Yang, that claims 1, 2, 4, 7, 11, and 13-15 are anticipated by US Patent 6,107,172 to Yang, and that claims 1, 2, 4, 7, 11, and 13-15 are anticipated by US Patent 6,283,131 to Chen.

The Examiner concedes that the etch recipes used in the present invention is not taught or suggested in any of these references or in any prior art reference on record. To overcome this deficiency, the Examiner relies upon US Patent 5,940,719 to Jang to demonstrate that "*etch recipes factors including the kinds, ratio and pressures of the etch gases and power are varied depending on the etch time (col. 5, 44-47)*".

The Examiner considers that this generic statement in Jang justifies that all differences in the etch recipe of the present invention are, therefore, rendered obvious.

Applicants disagree.

If the Examiner's evaluation were correct, then the Tao reference, the two Yang references, and the Chen reference would all be describing a technology below 100 nm, as required in the present invention. In fact, these reference fall short of achieving the dimension of 100nm or less of the present invention because their etch recipes are deficient to achieve this dimension, for the reason identified above that the ACLV is not maintained sufficiently to provide a successful etch at or below 100 nm.

That is, as clearly shown in Table 1 in column 5, Tao addresses 0.18 μm (180 nm) and 0.35 μm (350 nm). As explained in lines 33-54 of column 3, the Yang '651 recipe allows 0.18 μm (180 nm). As explained in lines 30-32 of column 6, the Chen recipe achieves only 0.15 μm (150 nm). In Yang '172, no target dimension is given. However, Applicants respectfully submit that the burden remains on the Examiner to demonstrate that the Yang '172 recipe satisfies the limitation that the target dimension is 0.1 μm (100 nm) or less.

In contrast, the inventors of the present invention have already achieved gatewidths as small as 0.04 μm (40 nm). This dimension is approximately one fourth of the best dimension explicitly cited in these prior art references.

The primary references used in the rejections are unable to achieve dimensions below their stated limits because these techniques fail to control the ACLV. It is for this reason that, even if the etch conditions in those references were continued in time, they would not achieve the critical dimension reached by the present invention.

Incidentally, this parameter is also the reason that claims 12 and 16 are directly related to claims 1-11 and 13-15 and the reason that Applicants traverse the Examiner's Restriction Requirement and have added new claims 17-20.

That is, in spite of the Examiner position articulated in the motivation to combine references, i.e., a motivation that seems to suggest that all etch recipes are equivalent, in order to achieve a critical dimension to a newer level, such as in the present invention, the etch recipe must be tuned to achieve a satisfactory ACLV for that critical dimension. The prior art references on record fail to provide a recipe for an etch that achieves this second aspect for the target critical dimension at or below 100 nm.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of " ... said higher resolution being 100 nm or less." For this reason alone, all claims are fully patentable over the cited references.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too, even in combination with Tao '440, Yang '651, Yang '172, Chen '131, Jang '719, or Bothra, fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview. The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

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